LIST OF CURRENT CLAIMS

1 (Currently Amended). A method for protecting a computer with a central processing unit (CPU) and a clock signal supply providing a clock signal to the CPU from external manipulation, comprising the steps of:

~~forming~~ determining a final check sum by mathematical combination with reference to register contents of the CPU arising at the end of processing of an instruction by the CPU,

storing the final check sum ~~and stored~~, and

~~forming~~ determining an initial check sum with reference to the register contents arising before the onset of processing of the next instruction by the CPU, and creating an error message if the initial check sum does not match the final check sum.

2 (Previously Presented). The method according to claim 1, wherein upon loading of the instruction a counter is started for counting clock cycles necessary for executing the instruction and outputting an error signal when the predetermined clock cycles are overshot or undershot.

3 (Previously Presented). The method according to claim 2, wherein the error signal triggers an interrupt or leads to discontinuance of the clock signal supply.

4 (Currently Amended). The method according to claim ~~1~~ 2, wherein the number of clock cycles necessary for executing an instruction is ~~obtained by a logic circuit~~ derived from the opcode of the instruction by a logic circuit.

5 (Previously Presented). The method according to claim 1, wherein the mathematical combination takes place by means of exclusive-OR combination of the register contents.

6 (Previously Presented). The method according to claim 1, wherein the initiation of the method is triggered by random or defined events.

7 (Previously Presented). The method according to claim 6, wherein the method is triggered in time-dependent fashion.

8 (Previously Presented). The method according to claim 6, wherein the method is triggered when the content of one or more registers of the CPU corresponds to a predetermined pattern.

9 (Currently Amended). The method according to claim 6, wherein the method is triggered after processing of a predetermined number of instructions ~~in each case~~.

10 (Currently Amended). A central processing unit (CPU) for a computer for carrying out the method according to claim 1, comprising:

[[-]]a combination of several registers of the CPU by logic elements to form a check sum,

[[-]]a check sum memory for storing a first check sum ~~formed~~ determined by the logic elements,

[[-]]a comparer for comparing a second check sum ~~formed~~ determined by the logic elements with the first check sum stored in the memory, and

[[-]]a control device for controlling the storage of the first check sum in the check sum memory and for controlling the comparer.

11 (Previously Presented). The central processing unit according to claim 10, including a counter for counting the clock cycles required for an instruction execution.

12 (Previously Presented). The central processing unit according to claim 10, including a logic circuit arranged to determine from the opcode of the instruction the clock cycles necessary for executing an instruction.

13 (Previously Presented). A computer comprising a central processing unit made according to claim 10.

14 (Previously Presented). A smart card comprising a central processing unit made according to claim 10.